

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Chi, et al.

Docket No.:

TSM03-0422

Serial No.:

10/718,920

Art Unit:

TBD

Filed:

November 21, 2003

Examiner:

TBD

For:

Modification of Carrier Mobility in a Semiconductor Device

Certificate of Mailing via First Class Mail (37 C.F.R. § 1.8(a))

Date of Deposit:

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Certificate of Mailing via First Class Mail (1 page)
Information Disclosure Statement (1 page)
IDS Form PTO/SB/08a and 08b (2 pages) citing (10) references
Copies of (9) cited references
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Respectfully submitted,

Natalie Swider Legal Assistant

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Tel: 972-732-1001 Fax: 972-732-9218

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Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants wish to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08a & 08b that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits.

Respectfully submitted,

March 11, 2004

Date

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PTO/SB/08a (08-03)

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	Substitute for form 1449A/PTC	,		Application Number	10/718,920	
	INFORMATION	DISCLO	SURE	Filing Date	11/21/2003	
	STATEMENT E	SY APPLI	CANT	First Named Inventor	Chi, et al.	
				Art Unit	TBD	
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Sheet	Sheet 1 of 2		Attorney Docket Number	TSM03-0422		

	U.S. PATENT DOCUMENTS								
Examiner Initials*	Cite No.1	Document Number Number - Kind Code ^{2 (if known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear				
	1	US-2003/0162348 A1	08-28-2003	Yeo, et al.					
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	FOREIGN PATENT DOCUMENTS									
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Substitu	ite for form 1449B/PTO			Complete if Known		
				Application Number	10/718,920	
INF	ORMATION DISC	a osi	IRF	Filing Date	11/21/2003	
STATEMENT BY APPLICANT (Use as many sheets as necessary)				First Named Inventor	Chi, et al.	
			-414.1	Art Unit	TBD	
				Examiner Name	TBD	
Sheet	2	of	2	Attomey Docket Number	TSM03-0422	

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	2	Rim, K., et al., "Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's," IEEE Transactions on Electron Devices, vol. 47, no. 7, pp. 1406-1415, July 2000.	
	3	Rim, K., "Strained Si Surface Channel MOSFETS for High-Performance CMOS Technology," IEEE International Solid-State Circuits Conference, paper #7.3, pp. 116-117, 2001.	
	4	Yeo, Y.C., et al., "Enhanced performance in Sub-100 nm CMOSFETs using Strained Epitaxial Silicon-Germanium," International Electron Device Meetings, pp. 753-756, 2000.	
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	6	Ito, S., et al., "Mechanical Stress Effect of Etch-Stop Nitride and Its Impact on Deep Submicron Transistor Design," International Electron Device Meetings, pp. 247-250, 2000.	
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	8	Ota, K., et al., "Novel Locally Strained Channel Technique for High Performance 55nm CMOS," International Electron Device Meetings, pp. 27-30, 2002.	
	9	Scott, G., et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress," International Electron Device Meetings, pp. 827-830, 1999.	
	10	Bianchi, R.A., et al., "Accurate Modeling of Trench Isolation Induced Mechanical Stress Effects on MOSFET Electrical Performance," International Electron Device Meetings, pp. 117-120, 2002.	

Examiner	Date	
Signature	 Considered	

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